REMARKS/ARGUMENTS

Upon entry of this amendment, which cancels claims 1-19, and adds new claims 20-38, claims 20-38 remain pending. Previously examined claims 1-19 were rejected under 35 U.S.C. 102(b) as being anticipated, or in the alternative, under 35 USC 103(a) as being obvious over USPN 5,511,013 to Tokieda et al. (hereinafter "Tokieda '013"). Consideration of the newly added claims in view of the comments below is respectfully requested. Applicants submit that newly added claims 20-38 are fully supported by the specification as originally filed and thus do not introduce new matter. It is noted here that the Office Action Summary sheet misidentifies, apparently inadvertently, the pending claims as claims 1-36 rather than claims 1-19. The Detailed Action section of the Office Action however properly addresses claims 1-19.

Claim Rejections

Claims 1-19 were rejected as anticipated by, or obvious in light of, Tokieda '013. Claims 1-19 have been cancelled and new claims 20-38 have been added. Applicants submit that the cancellation of claims 1-19 is not to be viewed as a concession on the merits of the rejection. Applicants further submit that claims 20-38 patentably distinguish over the cited reference.

Tokieda '013 teaches a microcomputer that receives "selection information 8" that is "indicative of use/non-use of" any one or more of multiple peripheral circuits. Col. 4, lines 57-67. The selection information is used to control the application of clock and address/data strobe signals to peripheral circuits. Col. 5, lines 13-33, and col. 5, line 66 to col. 6, line 9. By inhibiting the application of clock and strobe signals to unused peripheral circuits, power consumption in connection with the peripheral circuits is reduced. Col. 7, lines 7-20.

Applicants respectfully submit that disabling a peripheral circuit when not in use in order to save power as taught by Tokieda '013 is essentially what was described in general terms in the background section of the instant application. As also described in the background section of the instant application, problems may arise with systems of this type when the processor attempts to

access a peripheral circuit that has been disabled. That is, in prior art systems such as the one described in Tokieda '013, gating the clock or address/data strobe signals will disable a peripheral circuit from operating but will not necessarily inhibit the microprocessor from attempting to access the disabled peripheral circuit.

In the context of the microcomputer described by Tokieda '013, if CPU 3 attempts to access an unused peripheral circuit, it generates not only control signals such as address/data strobe signals, it may also generate address/data information that is placed on the ADDRESS/DATA BUS 5 intended for the unused peripheral circuit. The Tokieda '013 system teaches a mechanism for inhibiting the strobe signals and clock from reaching the unused peripheral circuit, but does not provide any mechanism for preventing the CPU 3 from attempting to access the unused peripheral circuit via ADDRESS/DATA BUS 5. That is, while an unused peripheral circuit in the Tokieda '013 system may be disabled because it does not receive a clock signal or strobe signals at its clock and strobe input terminals, the unused peripheral circuit may nevertheless receive address and data information from CPU 3 at its address/data input terminals coupled to ADDRESS/DATA BUS 5. When this happens, depending on the particular system, the system may experience an error condition with results which may not be predictable.

The present invention addresses this problem by providing an "address mapping logic" (26) that is separate from the "peripheral control register" (28) and provides different functionality. The peripheral control register controls the enabling and disabling of peripheral devices while the address mapping logic controls addressing of peripheral devices. "When the processor 12 wishes to transfer data on the bus 14, for example to one of the peripheral devices 16, 18, the address mapping logic 26 is used in order to determine the address to which that data must be transmitted." Page 4, lines 8-10. When a particular peripheral device is disabled by the peripheral control register, the address mapping logic modifies the address map to disable the address space allocated to that peripheral device. If the processor (12) attempts to access the disabled peripheral device, the modified address map will prevent the processor to do so in a

predictable fashion. Page 5, line 33 to page 6, line 8. All newly added claims recite "address mapping logic" or an "address map" that performs this functionality in combination with other elements including the disable logic.

Accordingly, independent claim 20 recites, *inter alia*, "address mapping logic coupled to the address map to automatically remove an address space allocated to a disabled peripheral device from the address map, whereby an address for the disabled peripheral device is not generated on the bus." Independent claim 28 recites, *inter alia*, "address mapping logic coupled to an address map for storing addresses allocated to the or each peripheral peripheral device to enable accesses thereto over said bus." Independent claim 35 recites, *inter alia*, " automatically removing from the address map the at least one address corresponding to the disabled peripheral device, thereby preventing further access attempts thereto via the bus."

Tokieda '013 fails to teach or suggest the claimed address map in combination with the other elements of the claims. In rejecting the previously pending (now cancelled) claims, the Examiner contends that register 17 in Tokieda '013 corresponds to the claimed address map. It is respectfully submitted that register 17 in Tokieda '013 cannot correspond to the claimed address map or address mapping logic for a number of reasons. First, register 17 stores "selection information 8" in the form of four single binary bits (171-174 wherein "1" signifies enable and "0" signifies disable) indicating the use/non-use of each of peripheral circuits 41, 42, 43 and 44, respectively. Tokieda '013 provides:

> Thus, in the second embodiment, by determining the selection information 8 to be supplied to the register 17 at the time of resetting the microcomputer, it is possible to select the peripheral circuits to which the clock 2 and the strobe signals 61, 62 and 63 are to be supplied, similarly to the first embodiment. In this connection, the use/non-use of the respective peripheral circuits 41, 42, 43 and 44 determined at the time of the resetting, namely, the logical value "1" or "0" of the respective bits 171, 172, 173 and 174 of the register 17 set at the time of the resetting, is not changed until a next resetting. Col. 6, lines 54-64.

Therefore, the bits stored in register 17 are not "address" bits for the peripheral circuits and instead indicate whether a particular peripheral device is in use or not in use. The actual address for the peripheral circuits 41-44 is provided by CPU 3 on ADDRESS/DATA BUS 5. Tokieda '013, col. 5, lines 35-38. There is therefore no address mapping function performed by register 17 of Tokieda '013.

Second, because register 17 does not store "addresses" for the peripheral circuits and performs no address mapping, there is no removing of an address space from register 17. As discussed above, register 17 stores four binary bits corresponding to four peripheral circuits. At all times register 17 stores four binary bits representing the use/non-use status of the four peripheral circuits. Thus, removing an address space as claimed by the present invention is not even relevant to the operation of register 17.

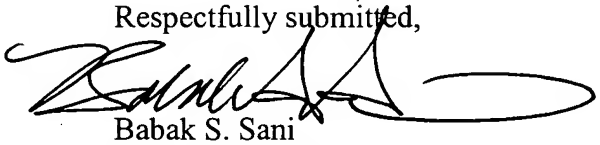
Thus, newly added independent claims 20, 28 and 35 are patentably distinguished over Tokieda '013 for at least the above reasons. The remaining dependent claims derive patentability from their respective independent claims and recite additional features that further distinguish over the cited reference. Applicants therefore submit that all newly added claims are patentable over the cited reference.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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